

1/4

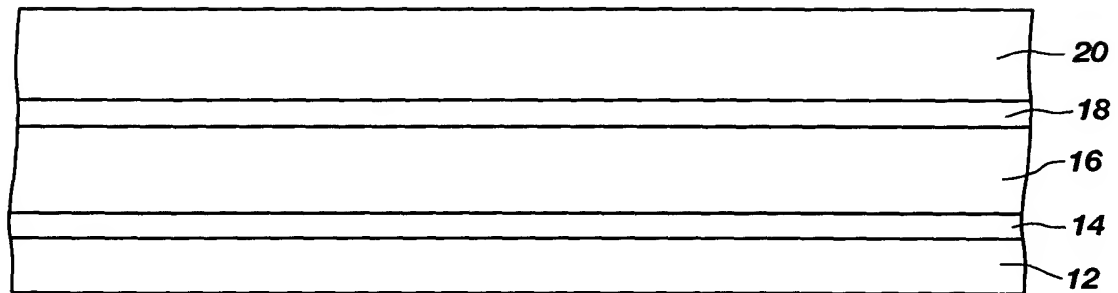


FIG. 1A

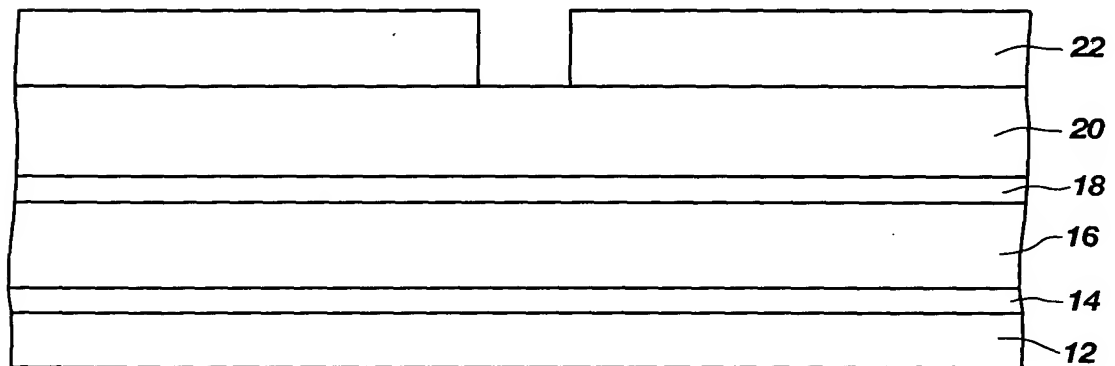


FIG. 1B

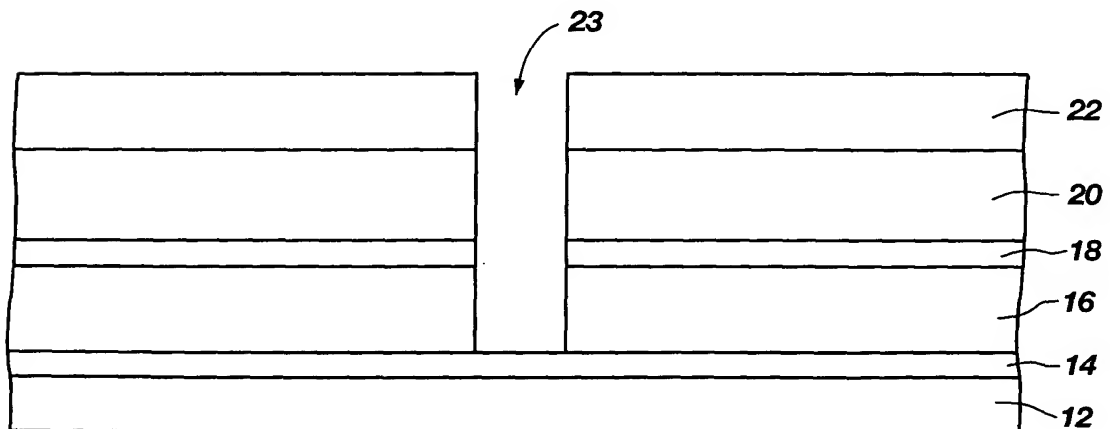


FIG. 1C

TITLE: METHOD FOR THE POST-ETCH CLEANING OF
MULTI-LEVEL DAMASCENE STRUCTURES HAVING
UNDERLYING COPPER METALLIZATION

Inventor: Michael T. Andreas

Serial No.: To Be Assigned

Docket No.: 2269-5981US

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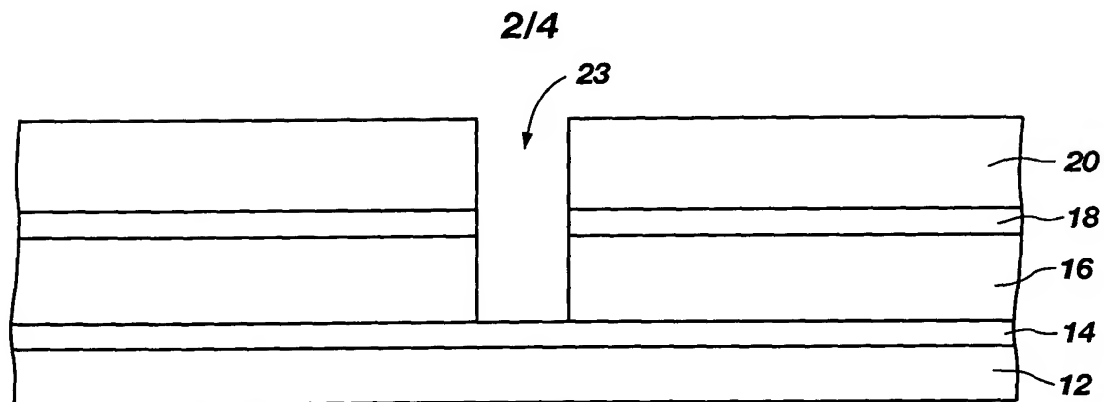


FIG. 1D

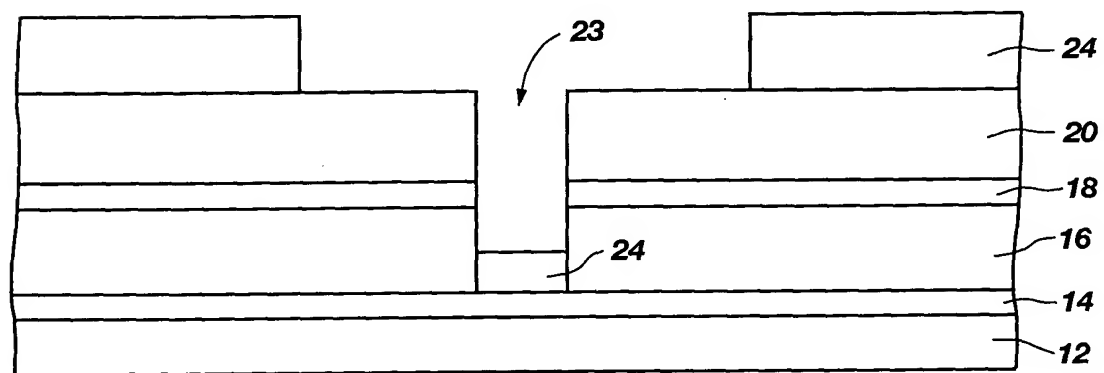


FIG. 1E

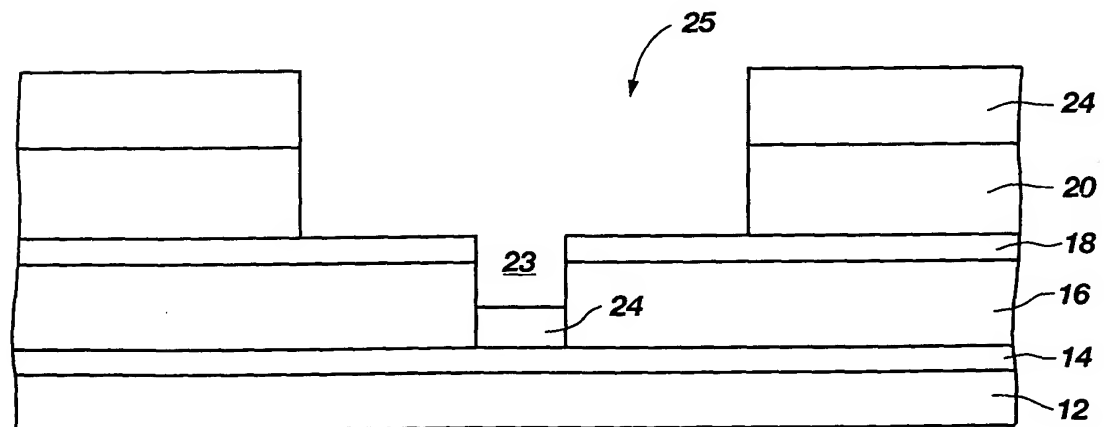


FIG. 1F

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A cross-sectional view of a semiconductor device. It shows a substrate 12 with a thin layer 14 on top. A trench 23 is formed in the substrate 12, extending through layer 14. The trench 23 is filled with a material 16. On the top surface of the device, there are two rectangular regions 20. The region on the right is labeled 25 with an arrow pointing to it. A thin layer 18 is located on the top surface of the device, covering the regions 20 and the top of the trench 23.

This cross-sectional view shows a semiconductor device with a central gap. The device consists of a substrate (12) with a base layer (14). Above the base layer is a layer (16) with a central opening (23). The opening is defined by side walls (23a). Above the side walls are two rectangular blocks (25a) separated by a gap (25). The top surface of the device is labeled 36. The layer (16) is also labeled 20.

A cross-sectional view of a semiconductor device. The device consists of a substrate 12 with a series of layers 14, 16, 18, 20, 26, 28, and 30. A central trench 23a is formed in the substrate, with side walls 25a on either side. The trench 23a is filled with a material, and the side walls 25a are also filled with a material. The layers 14, 16, 18, 20, 26, 28, and 30 are stacked on top of the substrate 12.

FIG. 11

4/4

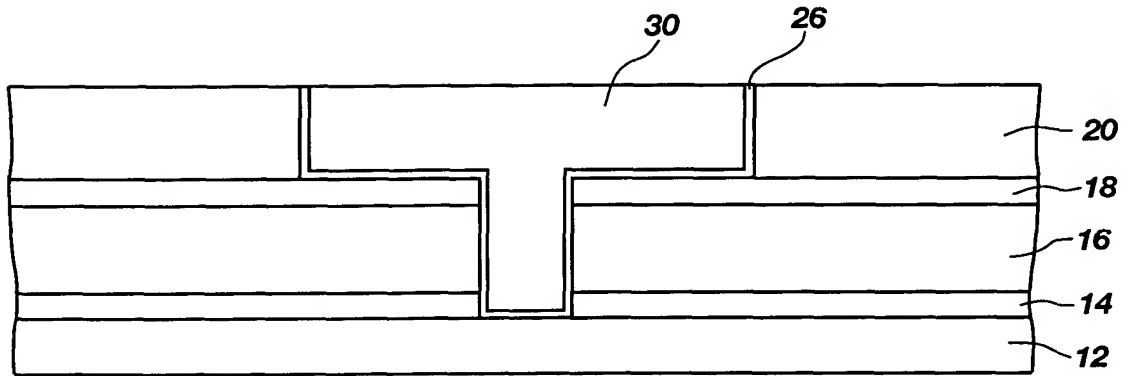


FIG. 1J

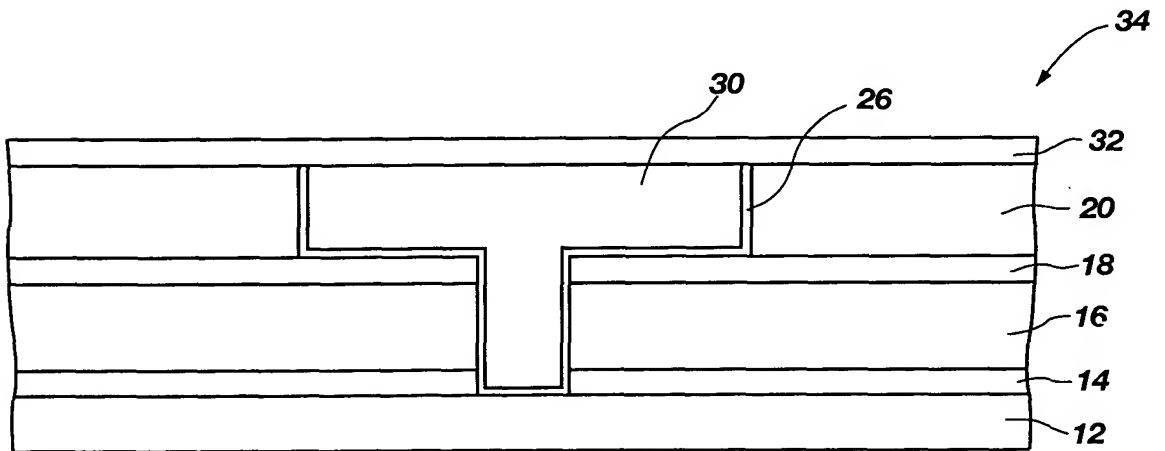


FIG. 1K